Module name: **Electrical Circuits 1**
Module ID: **IS-FEE-10070W**
Module type: **Specialization Workshop**
Semester: **winter 2024/2025**
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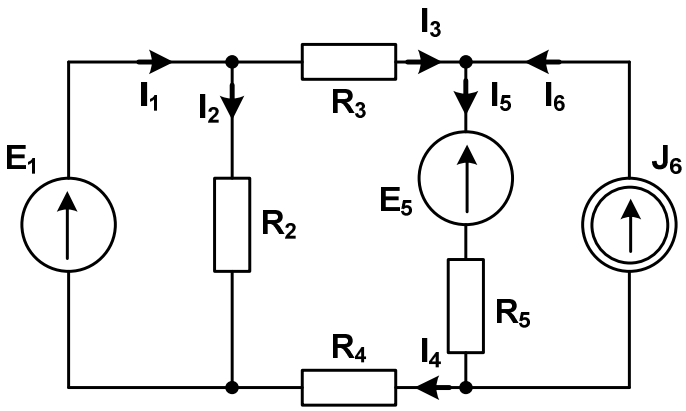
Workshop 02 (28.10.2024)

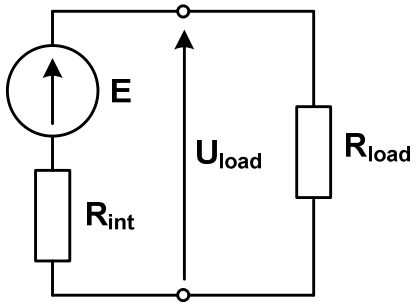
1. Calculate the currents in all branches of the circuit shown in the figure using the Loop-Current Method. Then, use the PSpice program to determine the currents in all branches of the same circuit, and compare these results with the calculations.

   $R_2 = R_3 = 10\ \Omega$, $R_4 = R_5 = 5\ \Omega$, $J_6 = 2$ A, $E_1 = 60$ V, $E_5 = 20$ V

   The report should include:
   - an electrical circuit diagram,
   - calculations of current values in all circuit branches,
   - an electrical circuit diagram (from the PSpice program) showing the determined current values,
   - conclusions: a comparison of calculation results with computer simulation results.



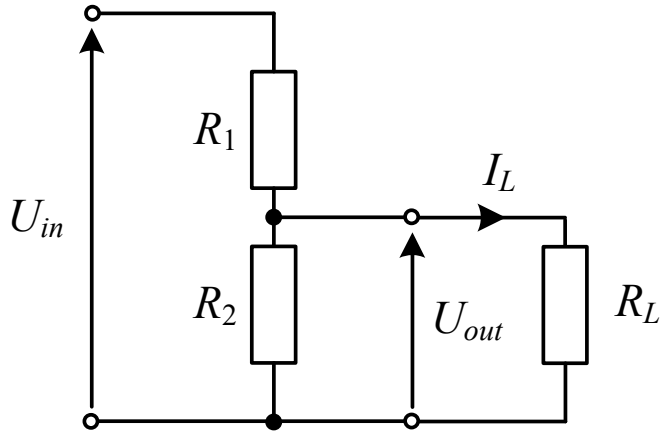
2. Maximum power transfer matching in a DC circuit occurs when the maximum power is transferred to the load (i.e., the load power reaches its maximum value). At this point, the voltage across the load is half of the source voltage. Using the PSpice program, perform a parametric analysis and plot the graphs $P_{load} = f(R_{load})$ and $U_{load} = f(R_{load})$.



   Assume $E = 9$ V, $R_{int} = 20\ \Omega$. Vary the resistance R_{load} from 1 to 50 Ω in increments of 1 Ω. Based on the obtained graphs, determine the R_{load} value at which the maximum power transfer occurs.

   The report should include:
   - an electrical circuit diagram and a simulation circuit diagram (from the PSpice program),
   - the graphs $P_{load} = f(R_{load})$ and $U_{load} = f(R_{load})$
   - conclusions: determination of the R_{load} value at which maximum power transfer occurs.

3. Design a voltage divider in which the output voltage U_{out} = ½ U_{in}. To do this, determine the values of resistors R_1 and R_2 from the E12 series (10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82) or their series or parallel combinations. Using the PSpice program, perform a parametric analysis and check whether, after connecting a load R_L to the divider, which varies from 1 kΩ to 5 kΩ, the output voltage U_{out} does not drop by more than 10% of its original value. If it does, adjust the values of R_1 and R_2 accordingly. Assume U_{in} = 9 V.



The report should include:

- an electrical circuit diagram and a simulation circuit diagram (from the PSpice program),
- the values of resistances R_1 and R_2,
- graphs $P_{out} = f(R_L)$,
- conclusions.